REMARKS

The present amendment is prepared in accordance with the new revised requirements of 37 C.F.R. § 1.121. A complete listing of all the claims in the application is shown above showing the status of each claim. For current amendments, inserted material is underlined and deleted material has a line therethrough.

Applicants appreciate the thoroughness with which the Examiner has examined the above-identified application. Reconsideration is requested in view of the amendments above and the remarks below.

No claims have been amended or added.

No new matter has been added.

Allowable Subject Matter

Applicants appreciate the thorough search conducted by the Examiner and the allowance of claims 21-30.

Applicants also note with appreciation the Examiner's comments that claims 33, 34, 36, 37 and 40 would be allowable if rewritten into independent form; however, applicants defer from doing so at this time for the reasons as set forth below.

No new matter has been added.

Specification

For purposes of placing the application in a condition for allowance, applicants have canceled incorporation of subject matter that was objected to in the parent application.

No new matter has been added.

35 USC § 102 Claim Rejections

The Examiner has rejected claims 31, 32, 35, 38 and 39 under 35 U.S.C. 102(c) as being anticipated by Chung (U. S. Patent No. 6,548,374). Applicants disagree.

It is submitted that independent claim 31, and as such claims 32-40 dependent thereon, are all directed to an isolation structure in a semiconductor substrate. This isolation structure includes a semiconductor substrate, a plurality of adjacent trenches in the semiconductor substrate, and a plurality of adjacent segments of the semiconductor substrate between each of the plurality of adjacent trenches. The isolation structure also includes an oxidation barrier layer residing in lower portions of the plurality of adjacent trenches. As claimed, the isolation structure of the invention has a self-aligned shallow trench isolation that is composed of merged sections of selected adjacent segments of semiconductor substrate, which are merged along a first row above the oxidation barrier layer.

Applicants submit that the present invention is not anticipated by Chung. Anticipation is but the ultimate or epitome of obviousness. To constitute anticipation, all material elements of a claim must be found in one prior art source. In re Marshall, 577 F.2d 301, 198 USPQ 344 (CCPA 1978).

Chung discloses defining a floating gate using a mask pattern 108 to form an oxide layer pattern 102, a first conductive layer pattern 104 and a nitride layer pattern 106 over a substrate 100. (Col. 5, ll. 44-47 and col. 6, ll. 1-21 and Figs. 3A-B.) The substrate 100 is etched using the mask pattern 108 to form trenches 109 such that the

floating gate is self-aligned with the active region. (Col. 6, ll. 22-34 and Fig. 3C.) Trench inner-wall oxide layer 110 is then deposited uniformly to a constant thickness. (Col. 6, l. 35 to col. 7, l. 8 and Fig. 3D.) Annealing is performed to obtain the densification of the trench inner-wall oxide layer 110 by forming an oxynitride layer 111 at the interface between the substrate 100 and the trench inner-wall oxide layer 110. (Col. 7, ll. 9-24.) A field oxide layer 124 is created inside the trenches 109 (Figs. 3E-F), followed by deposition of a polysilicon layer on the exposed first conductive layer pattern 104 and the field oxide layer 124. This polysilicon layer is then doped to form a second conductive layer in electrical contact with the first conductive layer pattern 104, which is then partially removed to form a second conductive layer pattern 126 for separating floating gates from those of neighboring cells. (Col. 7, l. 35 to col. 8, l. 24.)

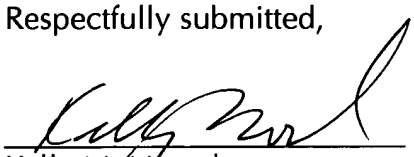
Applicants submit that the present invention is not anticipated by Chung. The isolation structure of the invention includes a self-aligned shallow trench isolation composed of merged sections of selected adjacent segments of semiconductor substrate. These sections of semiconductor substrate are merged along a first row above the oxidation barrier layer. As recited in dependent claim 38, the merged sections preferably comprise a thermal oxide region existing along the first row of selected ones of the plurality of adjacent trenches. Chung does not disclose or even suggest a self-aligned shallow trench isolation that is composed of merged sections of selected adjacent segments of semiconductor substrate, and as such, it does not disclose sections of thermal oxide region merged along a first row of selected plurality

of adjacent trenches as is currently claimed. Rather, Chung is limited to a floating gate that is self-aligned with the active region (col. 6, ll. 1-34, and Fig. 3A-C), whereby a field oxide layer 124 is created inside the trenches 109 and a second conductive layer pattern 126 is formed for separating floating gates from those of neighboring cells (col. 7, l. 35 to col. 8, l. 24 and Figs. 3E-F). It is submitted that Fig. 3D of Chung does not show, nor any other written text or figure, merged sections of semiconductor substrate100 along a first row above the oxidation barrier layer 111.

Since the present invention includes limitations that are neither disclosed nor contemplated by Chung, applicants submit that the present invention is neither anticipated by nor obvious over the Chung patent.

In view of the foregoing, applicants respectfully submit that the application has now been brought into a condition where allowance of the case is proper. Reconsideration and issuance of a Notice of Allowance are respectfully solicited. Should the Examiner not find the claims to be allowable, Applicants' attorney respectfully requests that the Examiner call the undersigned to clarify any issue and/or to place the case in condition for allowance.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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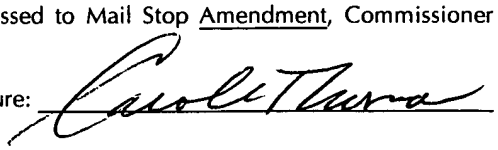

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